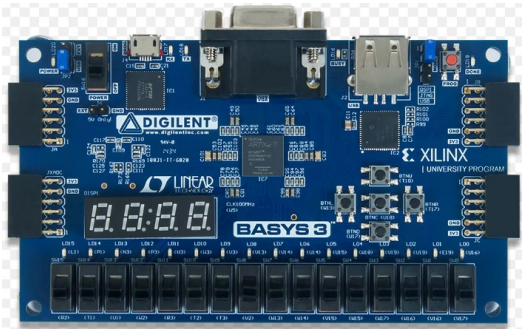
Chip Design Scholars
Networked Minds, Limitless Learning

Your final act: A high-impact Engineering program before the 2026 Early Action Deadline

The Program will be taught on industry-standard Basys 3 AMD Artix™ 7 FPGA Board

Shipped Kit includes

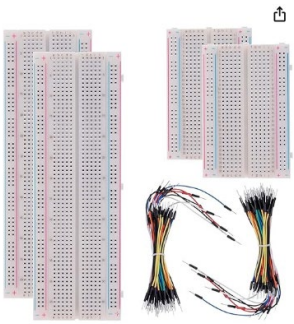
FPGA Board



Power Supply

Transistors, switches and LEDs

Breadboard and connectors



Program dates: August 2, 2026, to October 4, 2026 (in time for Early Action Deadline)

Timings: Typically, Sunday afternoon (Will not impact other activities)

Price: $1500 plus $250 deposit for kit

Note: Kits can be returned after the program or can be kept for $250

Certificate: Issued upon successful completion of the program

Sample Syllabus

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Week 1:

Basic intro, Logic gates, Binary system, Breadboarding, transistors

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Week 2:

Boolean algebra
Truth tables, K-maps Addition/subtraction [2's complement]
Combinational logic

Week 3:

Sequential logic
Flip-flops, counters, and clocks. Try tinkering around in Logisim
Timing - setup and hold, other important timing concepts

Week 4:

Intro to Verilog
How to code a simple design and verify it with a test bench
Learning how to use waveforms

Week 5:

Basics of memory, computer architecture

Week 6

Learning how to use an FPGA
Learn constraints (.xdc), synthesis, implementation, and bitstream generation.
Run a simple counter using the LED lights

Week 7:

Designing a Simple Digital System
Finite State Machines (FSMs)
Writing and verifying the design

Week 8:

Project kick-off. Will give guide rails and approaches. Have start implementing during the class

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Week 9:

Project implementation and debugging lab

Week 10:

ASIC flow overview

Final project presentations / Project overview:

The objective is to design and implement a digital reaction timer on the Basys 3 FPGA board. The system measures how quickly a user can respond to a visual stimulus (LEDs turning on) by pressing a physical push button. The final reaction time is accurately captured and displayed in milliseconds on the onboard 4-digit seven-segment display.

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